

LOW VOLTAGE OUTPUT DRIVE CIRCUIT

Fig. 1  
Fig. 2

BACKGROUND OF THE INVENTION

5 The present invention relates in general to electronic circuits and, more particularly, to depletion mode metal oxide semiconductor (MOS) devices in a series configuration.

10 Supervisor circuits find use in most if not all system supervisor applications. Systems requiring supervisor circuits are diverse and cover a wide range of uses from battery-powered equipment, computers, embedded systems, and microprocessor power supply monitoring. The  
15 supervisor circuit monitors a supply voltage and provides a reset signal to the microprocessor in the presence of a low supply voltage. If the supply voltage falls below some specified operating threshold the supervisor circuit triggers a reset of the microprocessor.

20 Typically, the supervisor circuit consist of a comparator to monitor changes in the supply voltage, and a trigger circuit to reset the microprocessor upon a supply voltage drop. If the comparator detects a change in supply voltage with respect to a voltage reference,  
25 the comparator sends a signal to the trigger circuit to reset the microprocessor.

As an example, a supervisor circuit monitors the supply voltage line of a microprocessor and compares the supply voltage to a voltage reference. If the supply  
30 voltage to the microprocessor drops below the voltage reference the supervisor circuit detects the voltage drop and resets the microprocessor, and puts the microprocessor in a fault mode. The microprocessor stays

in the fault mode until the supply voltage increases above the voltage reference, at which time the supervisor circuit removes the reset and the microprocessor thereafter operates in a normal mode.

5           The output of current prior art supervisor circuits have a state at which it can not guarantee an output if the supply voltage drops below some threshold voltage. The point below the threshold voltage at which the output of the supervisor circuit is not guaranteed is dependent upon the minimum voltage required to operate the trigger circuit. Typical implementations of a trigger circuit in the prior art are open drain or complimentary transistor configurations. Both of these configurations require a minimum voltage to be applied to the devices before the devices are operative. As a result, if the supply voltage to the microprocessor drops below the minimum voltage required to operate the trigger circuit, the output of the supervisor circuit can not be guaranteed and the microprocessor may inadvertently fall out of a fault mode. Also, for low voltage applications the supply voltage may operate close to the minimum voltage required to operate the trigger circuit, again resulting in an operation where the microprocessor may fall out of a fault mode.

25           Low voltage applications typically require linear regulators. A linear regulator takes in an unregulated input voltage and converts it to a regulated output voltage. The prior art typically uses an enhancement mode p-type transistor and a controller to provide the regulation. When the enhancement mode p-type transistor is turned off by the controller, there is some leakage current through the enhancement mode p-type transistor. The leakage current is typically inversely related to the

threshold voltage of the enhancement mode p-type transistor. Thus, you have to make the threshold voltage of the enhancement mode p-type transistor higher to reduce the leakage current. However, the input voltage must be at least the threshold voltage of the enhancement mode p-type transistor to turn the linear regulator on. Therefore, to operate a linear regulator at a low voltage results in a high leakage current through the device.

With advancing technology, most supply voltages to systems will drop down to the minimum voltage required to operate current prior art enhancement mode devices. For example, if the supply voltage of a microprocessor operates close to the minimum voltage required to operate the trigger circuit the microprocessor may experience inadvertent fault or operating modes. Furthermore, it would not be possible for a system to have a linear regulator operate at a low voltage with little or no leakage current using prior art enhancement mode devices. Thus, to meet advancing technology, a need exists for a circuit which can operate close to zero volts to replace trigger circuits presently used in prior art supervisor circuits to guarantee an output of the supervisor circuit for all input voltage levels. Also, the circuit must provide a linear regulator to operate in a low voltage environment without a high leakage current as seen with current prior art technology.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a supervisor circuit and microprocessor;

FIG. 2 is a waveform plot of an output signal of a prior art supervisor circuit;

FIG. 3 is a waveform plot of an output signal of a supervisor circuit; and

FIG. 4 is a schematic diagram of a trigger circuit of the supervisor circuit.

FIG. 5 is a block diagram of a prior art linear regulator circuit;

FIG. 6 is a block diagram of a linear regulator circuit;

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#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 illustrates one embodiment of system supervisor 10. Specifically, system supervisor 10 has supervisor circuit 12 to monitor a supply voltage line ( $V_{supply}$ ) of microprocessor 14. If  $V_{supply}$  drops below the minimum operating voltage of microprocessor 14, e.g. reset voltage threshold, microprocessor 14 is shut down via a reset signal sent by supervisor circuit 12. Upon reset, microprocessor 14 stays in a fault mode until  $V_{supply}$  increases above the reset voltage threshold for microprocessor 14.

In particular,  $V_{supply}$  is monitored at the input voltage ( $V_{in}$ ) of supervisor circuit 12. A voltage divider network receives the voltage at  $V_{in}$  and reduces the voltage by a ratio of resistor 16 and resistor 18. The reduced voltage is applied to the positive terminal of comparator 20. A reference voltage ( $V_{ref}$ ) is applied to the negative terminal of comparator 20. The reference voltage and resistor divider ratio are chosen based on the reset voltage threshold of microprocessor 14. If the voltage at the positive terminal of comparator 20 drops below  $V_{ref}$  at the negative terminal of comparator 20, an

output signal ( $V_c$ ) is sent to trigger circuit 22. Upon receiving the signal from comparator 20, trigger circuit 22 turns on, driving current through RL which provides a reset signal to microprocessor 14. Once microprocessor 14 receives the reset signal it falls into a fault mode. Microprocessor 14 stays in the fault mode until  $V_{supply}$  increases above the reset voltage threshold required for microprocessor 14 to operate in a normal mode.

FIG. 2 illustrates a plot of the transfer function of output voltage versus input voltage of a prior art supervisor circuit. FIG. 3 illustrates a plot of the transfer function of output voltage versus input voltage of supervisor circuit 12. In the prior art, a major problem with supervisor circuits is that the output voltage follows the input voltage when the input voltage is below some voltage  $V_{on}$ . As a result as illustrated in FIG. 2, a prior art supervisor circuit does not have a guaranteed output for an input voltage less than  $V_{on}$ . Voltage level  $V_{on}$  is representative of the voltage necessary to guarantee turn on of a trigger circuit of a prior art supervisor circuit.

The plot of the transfer function of output voltage versus input voltage of a supervisor circuit in FIG. 3 requires no minimum voltage to operate the trigger circuit. Thus, the supervisor circuit in FIG. 3 guarantees an output voltage for all input voltage levels to the supervisor circuit.

FIG. 4 illustrates trigger circuit 22 of supervisor circuit 12. Transistor 24 is a depletion mode transistor connected in a current source configuration to supply a small current  $I_{s1}$ . Transistor 24 has a source coupled to  $V_{in}$  to receive a voltage level,  $V_{supply}$ , a gate connected to the source of transistor 24, and a drain to supply  $I_{s1}$ .

Transistor 26 is an enhancement mode transistor, and receives a control signal ( $V_c$ ) to switch transistor 26 on and off with the output of comparator 20. Transistor 26 has a drain coupled to the drain of transistor 24 to receive  $I_{s1}$ , a gate coupled to  $V_c$  from comparator 20, and a source coupled to ground. Transistor 28 is an enhancement mode transistor, and switches on and off in response to  $V_c$ . Transistor 28 has a source coupled to receive  $V_{supply}$  at  $V_{in}$ , a gate coupled to the drain of transistor 26, and a drain coupled to the drain of transistor 30. Transistor 30 is a depletion mode transistor connected in a current sink configuration to supply small current  $I_{s2}$ . Transistor 30 has a drain coupled to the drain of transistor 28, a gate connected to the source of transistor 30, and a source coupled to ground. Transistor 32 is a depletion mode n-type transistor with a drain coupled to  $V_{out}$  of trigger circuit 22, and a gate coupled to the gate of transistor 28. Transistor 34 is a depletion mode p-type transistor with a source coupled to the source of transistor 32, a gate coupled to the drain of transistor 28, and a drain coupled to ground.

Trigger circuits used in the prior art typically consist of an inverter configuration with enhancement mode devices. FIG. 2 illustrates that a minimum voltage,  $V_{on}$ , is required in the prior art to operate the enhancement mode devices used in trigger circuits. The trigger circuit of FIG. 4 uses the depletion mode transistor pair 32, 34 to eliminate the requirement for a minimum  $V_{on}$ . In fact, using the depletion mode transistor pair 32, 34 in a trigger circuit provides down to a zero volt operation of a supervisor circuit.

In typical operation, trigger circuit 22 operates in

one of two states. If  $V_{supply}$  drops below the reset voltage threshold of microprocessor 14, the voltage at the positive terminal of comparator 20 drops below  $V_R$  at the negative terminal of comparator 20 and the output of comparator 20 goes low. A low output at  $V_c$  turns off transistor 26 causing drive current  $I_{s1}$  to charge the gate of depletion mode n-type transistor 32 pulling the gate voltage to  $V_{supply}$  keeping transistor 32 on. Transistor 28 turns off, allowing current  $I_{s2}$  to pull the gate of transistor 34 to ground keeping depletion mode p-type transistor 34 on. A current develops through load resistor 36 which creates a voltage drop  $V_{RL}$  that is subtracted from  $V_{supply}$  to provide a low output voltage at  $V_{OUT}$  of supervisor circuit 12. A low output at  $V_{OUT}$  of supervisor circuit 12 resets microprocessor 14 and puts microprocessor 14 in fault mode.

If  $V_{supply}$  is above the reset voltage threshold of microprocessor 14, then the voltage at the positive terminal of comparator 20 is greater than  $V_{ref}$  at the negative terminal of comparator 20 and the output of comparator 20 goes high. A high output at  $V_c$  turns on transistor 26 effectively driving current  $I_{s1}$  and the gate of transistor 32 to ground, turning transistor 32 off. Transistor 28 turns on and drives current  $I_{s2}$  from  $V_{supply}$  to ground setting the voltage at the gate of depletion mode p-type transistor 34 to  $V_{IN}$  which turns depletion mode p-type transistor 34 off. A high output at  $V_{OUT}$  of supervisor circuit 12 removes the reset from microprocessor 14 and puts microprocessor 14 in normal mode.

Depletion mode n-type transistor 32 and depletion mode p-type transistor 34 are driven by separate and independent control signals. To operate both of the

depletion mode devices independently requires that each gate thereof be driven by a separate source. Referring to FIG. 4, the gate of depletion mode n-type transistor 32 is driven by control signal  $V_{c1}$  at node N1, and the gate of depletion mode p-type transistor 34 is driven by control signal  $V_{c2}$  at node N2. Node N1 and N2 are separate and distinct sources supplying separate and distinct control signals. There is no necessary relationship between  $V_{c1}$  and  $V_{c2}$ .

To reset microprocessor 14, both depletion mode transistors are switched on. To switch both depletion mode transistors on, depletion mode n-type transistor 32 is driven by  $I_{s1}$  at node N1 to  $V_{supply}$  and depletion mode p-type transistor 34 is driven by  $I_{s2}$  at node N2 to ground. To remove the reset from microprocessor 14, both depletion mode transistors are switched off. To switch both depletion mode transistors off, transistor 26 is switched on driving  $I_{s1}$  at node N1 to ground resulting in zero volts applied to the gate of depletion mode n-type transistor 32, and transistor 28 is switched on driving node N2 and the gate of depletion mode p-type transistor 34 to  $V_{supply}$ .

FIG. 5 illustrates prior art linear regulator 40 using enhancement mode p-type transistor 42. Linear regulator 40 takes in an unregulated input voltage at  $V_{IN}$  and converts it to a regulated output voltage provided at  $V_{OUT}$ , and supplies a current at the regulated output voltage to load 46. Enhancement mode p-type transistor 42 has a gate voltage which is varied between  $V_{IN}$  and ground potential 43 by controller 44. During operation, when prior art enhancement mode p-type transistor 42 is turned off by controller 44, a leakage current develops through enhancement mode p-type transistor 42. Typically, to



reduce the leakage current, a larger threshold voltage for enhancement mode p-type transistor 42 is chosen to reduce the leakage current created at a zero gate to source voltage. However, the prior art poses the problem  
5 that as the threshold voltage is increased to compensate for the leakage current,  $V_{IN}$  must be at least the threshold voltage of enhancement mode p-type transistor 42 to turn linear regulator 40 on.

FIG. 4 illustrated an application using two  
10 depletion mode transistors, one n-type transistor and one p-type transistor with both transistors connected in series. The two depletion mode transistors have separate and distinct control signals applied to the gates thereof in a digital manner by a controller. In another  
15 application, two depletion mode transistors are controlled using separate and distinct control signals in an analog manner as explained forthcoming.

FIG. 6 illustrates linear regulator 50 using  
depletion mode transistor pair 52, 54 connected in  
20 series. Depletion mode transistor 52 is an n-type depletion mode transistor, and depletion mode transistor 54 is a p-type depletion mode transistor. Linear regulator 50 takes in an unregulated input voltage at  $V_{IN}$  and converts it to a regulated output voltage provided at  
25  $V_{OUT}$ , and supplies a current at the regulated output voltage to load 58. Controller 56 provides separate and independently controlled signals to the gates of each transistor thereof in an analog manner.

An n-type transistor by its physical characteristics  
30 typically has a lower current leakage than a p-type transistor. Using n-type depletion mode transistor 52 at the input,  $V_{in}$ , of linear regulator 50 controls leakage current thereof. Also, depletion mode transistors by

their inherent characteristic have a negative voltage threshold and as a result can operate at very low voltages. Linear regulator 50 uses the aforementioned characteristics of depletion mode transistors to provide regulation between  $V_{IN}$  and  $V_{OUT}$  at a low operating voltage without compromising leakage current.

Controller 56 provides continuous analog voltages, between zero volts and  $V_{IN}$ , to the gates of depletion mode transistor 52, and depletion mode transistor 54 to modulate the voltage at load 58, based on current at load 58. Depletion mode transistor 52, and depletion mode transistor 54 are driven by separate and independent control signals at the gates thereof by controller 56 to provide the load current necessary to regulate  $V_{OUT}$ . To operate both of the depletion mode devices independently requires that each gate thereof be driven by a separate source. Referring to FIG. 6, the gate of depletion mode n-type transistor 52 is driven by control signal  $V_{c3}$ , and the gate of depletion mode p-type transistor 54 is driven by control signal  $V_{c4}$ . Control signals  $V_{c3}$  and  $V_{c4}$  are separate and distinct sources supplying separate and distinct control signals. There is no necessary relationship between  $V_{c3}$  and  $V_{c4}$ .

Controller 56 includes amplifier 53 having a negative terminal connected between resistor 66 and resistor 64, a positive terminal connected to voltage reference 57, and an output connected to the gate of depletion mode transistor 52. Amplifier 55 has a positive terminal connected between resistor 60 and resistor 62, a negative terminal connected to a second voltage reference 59, and an output connected to the gate of depletion mode transistor 54. Resistors 60, 62, 64, and resistor 66 provide the necessary feedback information for controller

56.

In summary, a trigger circuit with the operation shown in FIG. 3 is illustrated to provide a guaranteed output for all input voltages down to zero volts. The trigger circuit is used within a supervisor circuit to monitor a microprocessor even if the operating voltage to the supervisor circuit drops to zero volts. In typical operation, if the operating voltage to a microprocessor drops below the reset voltage threshold of the microprocessor, which may be close to zero volts, the trigger circuit provides a reset signal to the microprocessor. When the operating voltage increases above the reset voltage threshold the trigger circuit removes the reset signal to the microprocessor. The trigger circuit consist of a depletion mode n-type and p-type transistor pair with their gates thereof driven by separate sources. The depletion mode n-type and p-type transistor pair are driven by separate sources to operate the transistor pair thereof out of phase to provide a logic function down to zero volts where the present art fails.

Furthermore, a linear regulator is shown in FIG. 6 with a depletion mode n-type and p-type transistor pair with their gates thereof driven by separate and distinct sources to provide a low voltage operation with minimal current leakage. The embodiment of FIG. 6 provides linear regulation for low voltage applications without compromise of leakage current. Having the n-type depletion mode transistor connected to  $V_{IN}$  further provides a low leakage current operation.

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